AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) A ~~one-bus~~ single memory bus multi-media computer system, comprising:

a CPU/Sound/Graphic unit connected to a program and sound bus and a graphic bus;

a bus arbitrator connected to said program and sound bus and said graphic bus on ~~one~~ a first side, and ~~said one-bus on the other~~ a single memory bus on a second side, said bus arbitrator including an address bus multiplexer for receiving a program and sound bus address and a graphic bus address as inputs, and outputting a single memory bus address, and a first data register for storing memory data from said single memory bus, said memory data being controlled by a bus control signal OEB for being temporarily stored in said first data register or directly outputted to a graphics data bus;

a program and sound and graphic memory connected to said ~~one-bus~~ single memory bus; and

a TV/LCD signal unit for outputting audio and video signals;

wherein said CPU/Sound/Graphic unit requests said program and sound and graphic memory by memory addresses, processes data returned from said program and sound and graphic memory, and sends [[the]] signals to said TV/LCD signal unit for outputting, said bus arbitrator sits between said CPU/Sound/Graphic and said program and sound and graphic memory to arbitrate [[said]] the memory requests from said CPU/Sound/Graphic unit to said program and sound and graphic memory.

2. (Currently Amended) The system as claimed in claim 1, wherein said ~~one-bus~~ single memory bus further comprises an address bus for sending address and a data bus for

sending data.

3. (Original) The system as claimed in claim 1, wherein said program and sound bus further comprises an address bus for sending address and a data bus for sending data.

4. (Original) The system as claimed in claim 1, wherein said graphic bus further comprises an address bus for sending address and a data bus for sending data.

5. (Currently Amended) The system as claimed in claim 1, wherein said bus arbitrator uses [[the]] a rule that a memory request to a faster memory is given a higher priority to access ~~the~~ said single memory bus without [[the]] pre-emptive capability.

6-7. (Cancelled).

8. (Currently Amended) The system as claimed in claim [[6]] 1, wherein said ~~second~~ bus control signal OEB controls the operation of said address multiplexer and said first data register with the following rules:

(a) when said ~~second~~ bus control signal OEB is low, said address bus multiplexer takes said graphics ~~second~~ bus address ~~and outputs one bus~~ for outputing said single memory bus address, at the same time, said first data bus register stores said ~~one bus~~ single memory bus data and outputs said [[first]] program and sound bus data;

(b) when said ~~second~~ bus control signal OEB is high, it is the accessing cycle for said [[first]] program and sound bus untill said ~~second~~ bus control signal OEB becomes low, during the accessing cycle of said [[first]] program and sound bus, ~~one bus~~ said single memory bus data is transported to said [[first]] program and sound bus data; and

(c) said ~~second~~ graphics bus gets said ~~second~~ graphics bus data before said ~~second~~

bus control signal OEB transits from low to high.

9. (Currently Amended) A system chip for processing audio and video data, comprising:

a CPU/Sound/Graphic unit connected to a program and sound bus and a graphic bus;

a bus arbitrator connected to said program and sound bus and said graphic bus on ~~one~~ a first side, and ~~said one bus on the other~~ a single memory bus on a second side, said bus arbitrator including an address bus multiplexer for receiving a program and sound bus address and a graphic bus address as inputs, and outputting a single memory bus address, and a first data register for storing memory data from said single memory bus, said memory data being controlled by a bus control signal OEB for being temporarily stored in said first data register or directly outputted to a graphics data bus;

a program and sound and graphic memory connected to said ~~one-bus~~ single memory bus; and

a TV/LCD signal unit for outputting audio and video signals;

wherein said CPU/Sound/Graphic unit requests said program and sound and graphic memory by memory addresses, processes data returned from said program and sound and graphic memory, and sends [[the]] signals to said TV/LCD signal unit for outputting, said bus arbitrator sits between said CPU/Sound/Graphic and said program and sound and graphic memory to arbitrate [[said]] the memory requests from said CPU/Sound/Graphic unit to said program and sound and graphic memory.